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1 A flat, timing-driven design system for a high-performance CMOS processor chipset
J. Koehl, U. Baur, T. Ludwig, B. Kick, T. Pflueger
February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(155.54 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe the methodology used for the design of the CMOS processor chipset used in the IBM S/390 Parallel Enterprise Server - Generation 3. The majority of the logic is implemented by standard cell elements placed and routed flat, using timing-driven techniques. The result is a globally optimized solution without artificial floorplan boundaries. We will show that the density in terms of transistors per mm2 is comparable to the most advanced custom designs and that the impact of interconnect d ...

2 Embedded hardware and software self-testing methodologies for processor cores
Li Chen, Sujit Dey, Pablo Sanchez, Krishna Sekar, Ying Cheng
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(103.87 KB) Additional Information: full citation, abstract, references, citings, index terms

At-speed testing of GHz processors using external testers may not be technically and economically feasible. Hence, there is an emerging need for low-cost, high-quality self-test methodologies, which can be used by processors to test themselves at-speed. Currently, Built-In Self-Test (BIST) is the primary self-test methodology available and is widely used for testing embedded memory cores. In this paper, we report our experiences in applying a commercial BIST methodology to two processor cor ...

3 Timing driven placement in interaction with netlist transformations
Guenter Stenz, Bernhard M. Riess, Bernhard Rohfleisch, Frank M. Johannes
April 1997 **Proceedings of the 1997 international symposium on Physical design**

Full text available: pdf(879.19 KB) Additional Information: full citation, references, citings, index terms

4 Topics in timing: Aggressive crunching of extracted RC netlists
Vasant B. Rao, Jeffrey P. Soreff, Ravichander Ledalla, Fred L. Yang
December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**

Full text available: pdf(344.60 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a *short-and-update* technique for resistors (*possibly connected to sinks*) that can further crunch the RC network effectively after eliminating *internal* nodes [1,14]. Our method produces a realizable RC circuit and preserves the total capacitance in the network. While our technique cannot guarantee preserving the Elmore delay at each network sink node, the maximum delay error can be controlled by the user. Our method provides a smooth tradeoff between run t ...

Keywords: RC reduction, TICER, crunching, elmore delay, interconnect modeling, node elimination, resistor shorting, time constants

5 Timing-driven placement for hierarchical programmable logic devices

Michael Hutton, Khosrow Adibsamii, Andrew Leaver

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Full text available: pdf(213.63 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we discuss new techniques for timing-driven placement and adaptive delay computation for hierarchical PLD architectures.Our algorithm follows the natural recursive k-way partitioning-based approach to placement on such devices. Our contributions include a specification of the overall TDC (timing-driven compilation) algorithm, an analysis of heuristics such as a variant of multi-start partitioning, a new method for adaptive delay computation, and a discussion of the ...

Keywords: CPLD, FPGA, algorithm, heuristic algorithm, partitioning, placement, programmable logic, timing-driven placement

6 Timing abstraction: Automated timing model generation

Ajay J. Daga, Loa Mize, Subramanyam Sripada, Chris Wolff, Qiuyang Wu

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(260.13 KB) Additional Information: full citation, abstract, references, index terms

The automated generation of timing models from gate-level netlists facilitates IP reuse and dramatically improves chip-level STA runtime in a hierarchical design flow. In this paper we discuss two different approaches to model generation, the design flows they lend themselves to and results from the application of these model generation solutions to large customer designs.

Keywords: EDA, model generation, static timing analysis

7 Timing driven placement for large standard cell circuits

William Swartz, Carl Sechen

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(56.96 KB) Additional Information: full citation, references, citings, index terms

8 Optimality and Stability Study of Timing-Driven Placement Algorithms

Jason Cong, Michail Romesis, Min Xie

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

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